Government of Karnataka

Department of Technical Education

Board of Technical Examinations, Bengaluru

Course Title: **Analog Electronics and Communication Lab**		Course Code	: **15EC35P**
Semester	: **Third**	Course Group	: **Core**
Teaching Scheme in Hrs (L:T:P)	: **0:2:4**	Credits	: **3**
Type of course	: **Tutorial + Practical**	Total Contact Hours	: **78**
CIE	: **25 Marks**	SEE	: **50 Marks**

Prerequisites

Basics of electrical and electronics engineering and semiconductor devices

Course Objectives

1. Use knowledge of BEEE and SCD to learn construction of regulated power supplies.
2. Study the working of BJT and operational amplifiers-based application circuits.
3. Demonstrate construction and verification of working of basic wave shaping circuits, filters and attenuators
4. Understand working of basic analog communication circuits like AM/FM modulation and demodulation

Course Outcomes

At the end of the course, the students will be able to attain the following Cos

Course Outcome		CL	Experiments linked	Linked PO	Teaching Hrs
CO1	Analyze the working of DC regulated power supplies	***U/A***	Unit-1: Part A: E1	1 to 10	**9**
CO2	Illustrate biasing of BJT as RC coupled CE amplifier and analyze its frequency response	***U/A***	Unit -1: Part A: E2	1 to 10	**6**
CO3	Analyze operations of Op-amp amplifier applications	***R/U/A***	Unit -1: Part A: E3-6	1 to 10	**15**
CO4	Illustrate construction and testing of Diode wave shaping circuits such as Clipper and Clamper.	***U/A***	Unit -1: Part A: E7-8	1 to 10	**6**
CO5	Observe the correctness of maximum power transfer theorem and behavior of resonant circuits,	***R/U/A***	Unit -1: Part B: E1-2	1 to 10	**12**
CO6	Analyze the circuit diagrams of filters and attenuators, AM & FM modulation and demodulation	***R/U/A***	Unit -1: Part A: E3-7	1 to 10	**15**
				CIE/IA assessment tests	**06**
				Total	**69**

Legend: E- Experiment, R-Remember, U-Understand, A-Application, CL-Cognitive Level, PO-Program Outcome
Note: Total sessions include two tests

Course-PO Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Analog electronics and communication lab	3	3	3	3	3	--	--	3	1	3

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3

If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2

If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1

If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

Course Contents

Unit – 1: Tutorial and Graded Exercises 69 Hours

Sl. No	Topic / Exercises	Duration (Hr.)
	Part- A	
1	Construct a regulated power supply to generate 12V and note down the voltage/waveform at each stage (Use discreet components/ ICs for sub circuits)	9
2	Construct voltage divider biased single-stage RC coupled CE amplifier and plot frequency response	6
3	Construct and verify Inverting or non inverting amplifier using Op-amp	3
4	Construct and verify summing or difference amplifier using Op-amp	3
5	Construct and verify differentiator or integrator amplifier using Op-amp	3
6	Construct and verify RC phase-shift oscillator circuit using Op-amp	6
7	Construct and test a positive or negative clipper circuit	3
8	Construct and test positive or negative clamper circuit	3
	Part-B	
1	Verification of maximum power transfer theorem.	6
2	Plot the frequency response of series resonant circuit and find its bandwidth and Q factor	6
3	Construct and test the passive low-pass T-type filter circuit for a give cut-off frequency	3
4	Construct and test active high-pass filter using Op-amp for a given cut-off frequency and gain	3
5	Construct and test PI type attenuator circuit for the given attenuation & Ro	3
6	Construct and verify amplitude modulation and demodulation using trainer kits	3
7	Construct and verify frequency modulation and demodulation using trainer kits	3
	Conduction of CIE/IA tests	6
	Total	69

Unit – 2: Projects/ Activities [CIE- 05 Marks] 9 Hours

Activity
Prepare module from the list below by placing the components in the General PCB / copper-clad sheet and soldering/wired connection (1) +12v power supply, (2) -12v power supply, (3) +5v power supply, (4) -5v power supply, (5) Half-wave and Full-Wave Rectifier, (6) Half-wave and Full-Wave Rectifier with filter (7) Voltage regulator using Zener diode, (8) Voltage regulator using transistor and op-amp (9) Single stage voltage divider bias RC coupled amplifier, (10) Two stage voltage divider bias RC coupled amplifier, (11) Inverting Amplifier, (12) Non-Inverting amplifier, (13) Inverting Summing Amplifier using op-amp, (14) Non-Inverting Summing Amplifier using op-amp (15) Difference amplifier using op-amp, (16) Differentiator using op-amp, (17) Integrator using op-amp, (19) Comparator using op-amp, (20) Zero cross detector using op-amp, (21) Instrumentation amplifier

Institutional Activity (No marks)

The following are suggested institutional activities. At least one activity or similar activity can be carried out during the semester. The course teacher/coordinator is expected to maintain the relevant record (Containing, Activity name, Resource persons and their details, duration, venue, student feedback, etc) pertaining to Institutional activities.

Sl. No.	Activity
1	A seminar of electronics equipment handling and Lab maintenance
2	A visit to electronics industry/ electronics research labs
3	Organize hands-on practice to construct an application specific module

References

1. *Electronics laboratory primer*, S. Poorna Chandra, B. Sasikala, S. Chand Technical Publication. ISBN 81-219-2459-6
2. *Fundamentals of Electronic Devices and Circuits Laboratory Manual* ,David A. Bell Oxford University Press, ISBN 978-0-19-542988-6
3. *Electronic Devices,* Thomas L Floyd,ISBN10: 8177586432

Course Delivery

The course will be delivered through tutorials of two hours and four hours of hands on practice per week. Student activities are off-class and

Course Assessment and Evaluation Scheme

Master Scheme

Assessment Method	What		To Whom	Assessment mode /Frequency /timing	Max. Marks	Evidence Collected	Course Outcomes
Direct assessment	CIE	IA	Students	Two tests+	**10**	Blue Books	1 to 6
				Record@	**10**	Record Book	1 to 6
				Activity*	**05**	Report/Sheets	1 to 6
	SEE	End exam		End of the course	**50**	Answer Scripts at BTE	1 to 6
				Total	**75**		
Indirect assessment	Student feedback on course		Students	Middle of the Course	Nil	Feedback Forms	1 to 3 Delivery of course
	End of course survey			End of the Course	Nil	Question-naires	1 to 6 Effectiveness of delivery instructions & assessment methods

Legends: CIE-Continuous Internal Evaluation, SEE- Semester End-exam Evaluation

+ I.A. test shall be conducted as per SEE scheme of valuation. However obtained marks shall be reduced to 10 marks. Average marks of two tests shall be rounded off to the next higher digit.
Rubrics to be devised appropriately by the concerned faculty to assess Student activities.

***S**tudents should do activity as per the list of suggested activities/ similar activities with prior approval of the teacher. Activity process must be initiated well in advance so that it can be completed well before the end of the term.

@ Record Writing: Average of marks allotted for each experiment; fractional part of average shall be rounded-off to next higher integer.

Composition of CLs

Sl. No.	Cognitive Levels (CL)	Weightage (%)
1	Remembering	20
2	Understanding	30
3	Applying	50
	Total	**100**

Continuous Internal Evaluation (CIE) pattern

(i) Student Activity (5 marks)

The student activities in Unit-2 or similar activities can be assigned

Execution Notes:

1. Activities are assigned batch-wise (maximum of 2 students per batch); any one activity/project per batch should be assigned by the teacher based on interest of the students. Student can also choose any other similar activity with a prior approval from the concerned teacher.
2. Teacher is expected to observe and record the progress of students' activities
3. Assessment is made based on quality of work as prescribed by the following **rubrics** table.

(ii) Model of rubrics for assessing student activity (for every student)

Dimension	Scale					Marks (Example)
	1 Unsatisfactory	2 Developing	3 Satisfactory	4 Good	5 Exemplary	
1. Research and gathering information	Does not collect information relate to topic	Collects very limited information, some relate to topic	Collects basic information, most refer to the topic	Collects more information, most refer to the topic	Collects a great deals of information, all refer to the topic	3
2. Full-fills team roles and duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs almost all duties	Performs all duties of assigned team roles	2
3. Shares work equality	Always relies on others to do the work	Rarely does the assigned work, often needs reminding	Usually does the assigned work, rarely needs reminding	Always does the assigned work, rarely needs reminding.	Always does the assigned work, without needing reminding	5
4. Listen to other team mates	Is always talking, never allows anyone to else to speak	Usually does most of the talking, rarely allows others to speak	Listens, but sometimes talk too much,	Listens and talks a little more than needed.	Listens and talks a fare amount	3
					Total marks	ceil(13/4)= 4

(iii) CIE/IA Tests (10 Marks)

Two tests have to be conducted in accordance SEE pattern and the marks shall be scaled down to 10. Average of two tests, rounding-off any fractional part to next higher integer, shall be considered for CIE/IA.

(iv) Record Evaluation (10 Marks)

Every experiment shall be assigned marks, in the scale of 10, after its conduction based on student's performance and quality of write-up. Average of them, by rounding-off any fractional part to next higher integer, shall be considered for CIE/IA.

Semester End-exam Evaluation (SEE) Scheme

Sl. No.	Scheme	Max. Marks
1	Writing two specified circuits/diagrams (one each from part A and part B) with applicable Procedure / Tabular Col./ Ideal graph/ formula calculations	15
2	Construction and conduction of any one circuit	20
3	Result	05
4	Viva-voce	10
TOTAL		**50**

Note:

1. Equal weightage for Part A and Part B experiments
2. Candidate is expected to submit the Lab record for the examination
3. Student shall not be allowed to conduct directly if he/she is unable to write at least one correct circuit diagram

Laboratory Resource Requirements

Hardware Requirement for a batch of not more than 20 students

Sl. No.	Equipment	Approx. Quantity
1	Regulated Power supply (1A/2A, 0-30V)	10
2	DC Voltage supply (+/-5v, +/-12V, +/-15V)	10
3	Dual trace oscilloscope (upto 20 to 30MHz)	10
4	Digital multi-meters	10
5	Function/Signal generators	10
6	Amplitude modulation and Demodulation kits	05
7	Frequency modulation and Demodulation kits	05
8	Step down transformer, Capacitors, Resistors, Inductors, BJT, Op-amp IC-741, Regulator IC-7812, Diode	Consumables
9	Single strand wire/Patch cards (different lengths), probes	
10	Bread board / Analog trainer kit	10

Model Questions for Practice and Semester End Examination

Note: These questions are indicative but not exhaustive.

1. Construct a part of regulated power supply to generate 12V supply and measure/record the voltage/waveform at each stage (Using discreet component) (Suggestion: assign only subcircuits of RPS, executable in 3hrs)
2. Construct of voltage divider biased single stage RC coupled CE amplifier and plot frequency response.
3. Construct and verify inverting or non inverting amplifier using Op-amp for gain of 10
4. Construct and verify Summing or Difference amplifier using Op-amp square/sine wave input
5. Construct and verify Differentiator or integrator amplifier using Op-amp for square/sine wave input.
6. Construct and verify RC phase shift oscillator circuit using Op-amp to oscillate at 200Hz
7. Construct a positive or negative clipper circuit and record its output for a given input
8. Construct and verify the functioning of positive or negative clamper circuit
9. Verify of the correctness of maximum power transfer theorem
10. Plot the frequency response characteristics of series resonant circuits and find their Bandwidth and Q factor.
11. Construct and test circuit of passive Low pass filter T-type for cut-off freq f_1 Hz
12. Construct and test Active High pass filter using op-amp for a cut-off frequency f_1 Hz
13. Design and construct PI attenuator circuit for the given attenuation & Ro
14. Generate amplitude modulated signal and recover the modulating signal from it experimentally
15. Generate frequency modulated signal and recover the modulating signal from it experimentally

End